

# Reconfiguration Of VLSI Arrays By Covering (Technical Report. Texas A & M University. Computer Science Dept) By Fabrizio Lombardi

By Fabrizio Lombardi

## VLSI09\_Proceedings - Ace Recommendation Platform - -

Subjects VLSI Design Digital Systems and VLSI. VLSI09\_Proceedings. Document Information; Type: Lecture Notes; Total # of pages: 599. Avg Rating:

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## Patent US7412586 - Switch memory architectures - -

The present invention provides a switch memory architecture (SMA) consisting of: (i) processing elements (PE) (ii) memory banks (MB), and (iii) interconnect switches

<http://www.google.com/patents/US7412586>

## Design, analysis and reconfiguration of -

U of I Only Design, analysis and reconfiguration of defect-tolerant VLSI and parallel processor arrays

<https://www.ideals.illinois.edu/handle/2142/19803>

## Radzihovsky, Leo - ml-struct-svm -

Texas AM University School Dept. of Physics Vanderbilt University, Dept. of Loughborough University ( Department of Computer Science and

<http://ml-struct-svm.googlecode.com/svn-hist/trunk/DataSet/Dmoz/raw-dataset/preprocessing/dataset-24.xml>

## Dirk Stroobandt | Computer Systems Lab -

Computer Systems Lab (CSL) - HES (Hardware and Embedded Systems) team Electronics and Information Systems (ELIS) department Ghent University Sint Pietersnieuwstraat 41

<http://csl.elis.ugent.be/dstrooba>

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## Patent US8471593 - Logic cell array and bus system -

A logic cell array having a number of logic cells and a segmented bus system for logic cell communication, the bus system including different segment lines having

<http://www.google.co.uk/patents/US8471593>

## ISSUU - UCONN Engineering Annual Report 2009-2010 -

Annual Report

<http://issuu.com/uconn-engineering/docs/annual-report-2009-10>

**1 Session A03 RF and Microwave Standards; -**

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<http://www.docstoc.com/docs/87470064/1-Session-A03-RF-and-Microwave-Standards;-Realisation-and->

**www.cs.cmu.edu -**

%0 Generic %T TRW Monolithic Video A/D Converter %0 Book %D 1979 %T The 8086 Family User's Manual %0 Book %D 1988 %T Programming Parallel Processors %I Addison-Wesley

<http://www.cs.cmu.edu/afs/cs.cmu.edu/user/webb/html/PCV.ref>

**On designing ULM-based FPGA logic modules -**

Department of Computer Sciences, University of Texas at Austin: Technical Report UCB/ERL M92/41, Dept. of Electrical Engg. and Computer Science,

<http://dl.acm.org/citation.cfm?id=201311&dl=ACM&coll=DL>

**Computer-Aided Design of Integrated Circuits and -**

Lombardi, Fabrizio; In VLSI arrays, redundant cells are added as spares. Dept. of Computer Science. and Engineering. 354D IST Building.

<http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=1482>

**Fault Tolerance Through Reconfiguration in VLSI -**

Fault Tolerance Through Reconfiguration in VLSI and WSI Arrays (Computer Systems Series) Hardcover February 9, 1989

<http://www.amazon.com/Tolerance-Through-Reconfiguration-Computer-Systems/dp/0262140446>

**Reconfiguration of high performance VLSI sub- -**

Reconfigurable techniques attempt to realise maximum possible fault-free sub-arrays in mesh connected VLSI arrays with faulty elements. Although this problem has been

[http://digital-library.theiet.org/content/journals/10.1049/ip-cds\\_20050273](http://digital-library.theiet.org/content/journals/10.1049/ip-cds_20050273)

**CiteSeerX Testing and Reconfiguration of VLSI -**

BibTeX @MISC{Prisco98testingand, author = {Roberto De Prisco and Angelo Monti and Linda Pagli}, title = {Testing and Reconfiguration of VLSI Linear Arrays}, year

<http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.50.1433>

**www.google.com -**

www.google.com

<http://www.google.com/patents/US20070198971>

**Efficient reconfiguration of VLSI arrays - -**

We consider the problem of reconfiguring a 2-dimensional VLSI array with faulty cells. A network flow model of the problem is formulated and an algorithm is presented

<http://link.springer.com/chapter/10.1007%2FBFb0040387>

**Reconfiguration of VLSI arrays by covering ( -**

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<http://www.amazon.co.uk/Reconfiguration-covering-Technical-University-Computer/dp/B00071G3XK>

**PgroupW - User contributions [en] -**

This cyberphysical domain provides unique challenges to many existing computer science algorithms, approaches and frameworks due to the data complexity,

<http://ganges.usc.edu/pgroupW/index.php?title=Special:Contributions/Saman&feed=atom&limit=50&target=Saman&year=&month=>

**www.ifis.uni-luebeck.de -**

388-391 2002 conf/ah/2002 AH db/conf/ah/ah2002.html#BraASS02 Maria A. M. Souto Regina Verdin

<https://www.ifis.uni-luebeck.de/lehre/ws0506/dbs2/uebl2/tinyDbIpl.xml>

**www.worldcat.org -**

integration 1988 Technical report ; 1988 en 18647828 18647828 Reconfiguration of VLSI arrays by covering Sami Texas A & M University. Computer Science Dept

<http://www.worldcat.org/oclc/18647828.rdf>

**ISSUU - School of Engineering Lab Activity Report -**

School of Engineering Lab Activity Report 2009. John Maxwell Follow publisher. Be the first School of Engineering Lab Activity Report 2009.

<http://issuu.com/epfl/docs/publicversion>

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<http://www.amazon.co.uk/Fabrizio-Lombardi/e/B00JVGLYDQ>

**Advanced Data Layout Optimization for Multimedia -**

Technical Report, University of Wisconsin, Lecture Notes In Computer Science The computational model considered is the arrays with a reconfigurable

<http://dl.acm.org/citation.cfm?id=662819>

**Patent US8127061 - Bus systems and reconfiguration -**

A processor chip includes data processing elements that each has dedicated to it a respective switch for dynamically establishing an interconnection between the data

<http://www.google.com/patents/US8127061>

**Items in bibliography identified by a string -**

Vanderbilt University .See of Cambridge Computer Laboratory Technical Report Technical Symposium on Computer Science

<http://www.csci.csusb.edu/dick/bibfull.php?from=bib&search=COMPUTER>

**Reconfiguration of VLSI arrays: a technique for -**

The problem afforded is that of dynamic reconfiguration of regular arrays of processing elements, implemented as VLSI devices; the aim is that of achieving high

<http://www.sciencedirect.com/science/article/pii/0165607485900468>

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<http://www.amazon.com/Fabrizio-Lombardi/e/B00JVG1YDQ>

**Reconfiguration of VLSI arrays by covering - IEEE -**

In VLSI arrays, redundant cells are added as spares. The proposed approach is applicable as an offline technique at either production time and/or run time.  
<http://ieeexplore.ieee.org/xpl/articleDetails.jsp?reload=true&arnumber=35547>

**Patent US8230411 - Method for interleaving a -**

Patent US8230411 - Method for interleaving a program over a  
<http://www.google.com/patents/US8230411>

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2 Department of Computer Science and Electrical Engineering, Dept. of Electrical and Computer Engineering, M. Stankus. VSB - Technical University of Ostrava,  
[http://www.auth.gr/sites/default/files/press/conference\\_programm-26-5-2010.doc](http://www.auth.gr/sites/default/files/press/conference_programm-26-5-2010.doc)

**Patent US8156312 - Processor chip for -**

Patent US8156312 - Processor chip for reconfigurable data  
<http://www.google.com/patents/US8156312>

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file{ %%% author = "Nelson H. F. Beebe", %%% version = "2.91

<http://www.netlib.org/tex/bib/super.bib>

**Fault-tolerance through reconfiguration of VLSI -**

Get this from a library! Fault-tolerance through reconfiguration of VLSI and WSI arrays. [R Negrini; Mariagiovanna Sami; Renato Stefanelli]

<http://www.worldcat.org/title/fault-tolerance-through-reconfiguration-of-vlsi-and-wsi-arrays/oclc/18290085>

**Testing and reconfiguration of VLSI linear arrays -**

Achieving fault tolerance through incorporation of redundancy and reconfiguration is quite common. In this paper we study the fault tolerance of linear arrays o

<http://www.sciencedirect.com/science/article/pii/S0304397597002387>

**Patent US8209653 - Router - Google Patents -**

Configuration of reconfigurable multidimensional fields are described. Information is provided for handling feedback, among other things.

<http://www.google.co.ug/patents/US8209653>

**Reconfiguration of VLSI arrays by covering (Book, -**

Reconfiguration of VLSI arrays by covering. [Fabrizio Lombardi; > # Reconfiguration of VLSI arrays by covering Texas A & M University. Computer Science Dept

<http://www.worldcat.org/title/reconfiguration-of-vlsi-arrays-by-covering/oclc/18647828>

**On the Reconfiguration Algorithm for -**

In this paper, an improved algorithm is presented for the NP-complete problem of reconfiguring a two-dimensional degradable VLSI array under the row and column  
[http://link.springer.com/chapter/10.1007/3-540-44863-2\\_36](http://link.springer.com/chapter/10.1007/3-540-44863-2_36)

**On the reconfiguration of degradable VLSI/WSI -**

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